

## PUSH-PULL FOUR CHANNEL DRIVER WITH DIODES

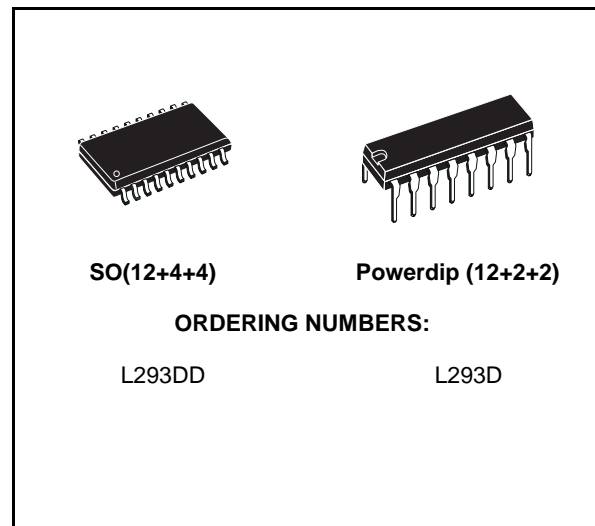
- 600mA OUTPUT CURRENT CAPABILITY PER CHANNEL
- 1.2A PEAK OUTPUT CURRENT (non repetitive) PER CHANNEL
- ENABLE FACILITY
- OVERTEMPERATURE PROTECTION
- LOGICAL "0" INPUT VOLTAGE UP TO 1.5 V (HIGH NOISE IMMUNITY)
- INTERNAL CLAMP DIODES

### DESCRIPTION

The Device is a monolithic integrated high voltage, high current four channel driver designed to accept standard DTL or TTL logic levels and drive inductive loads (such as relays solenoids, DC and stepping motors) and switching power transistors.

To simplify use as two bridges each pair of channels is equipped with an enable input. A separate supply input is provided for the logic, allowing operation at a lower voltage and internal clamp diodes are included.

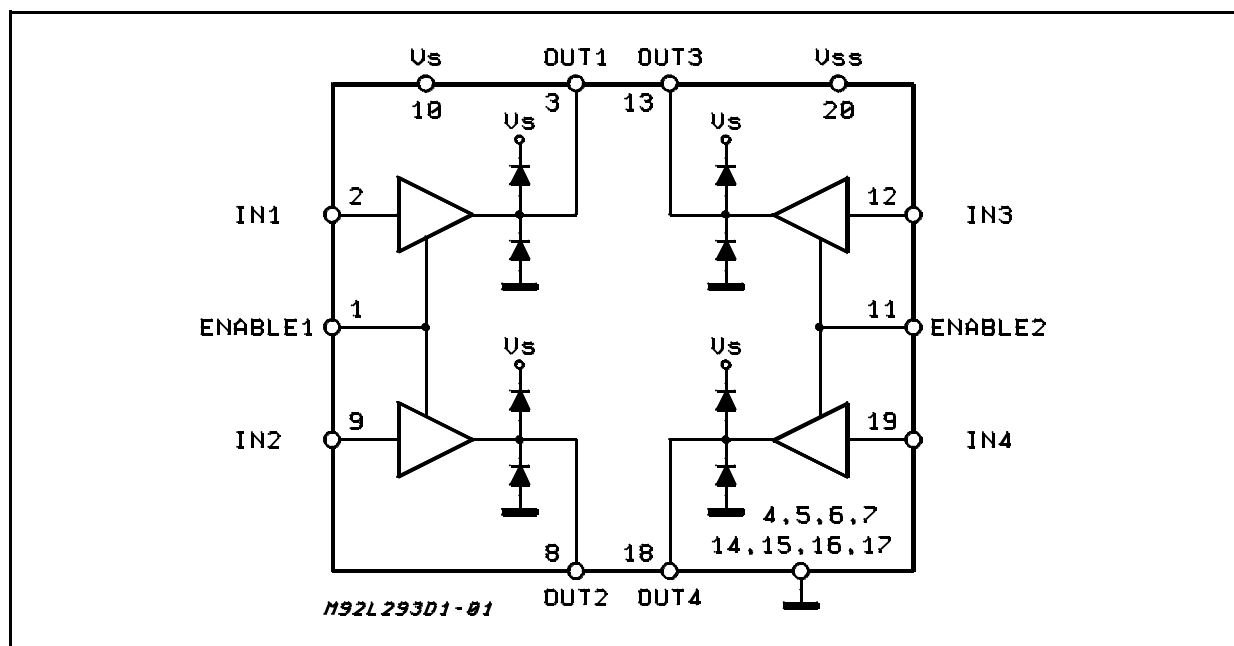
This device is suitable for use in switching applications at frequencies up to 5 kHz.



The L293D is assembled in a 16 lead plastic package which has 4 center pins connected together and used for heatsinking

The L293DD is assembled in a 20 lead surface mount which has 8 center pins connected together and used for heatsinking.

### BLOCK DIAGRAM

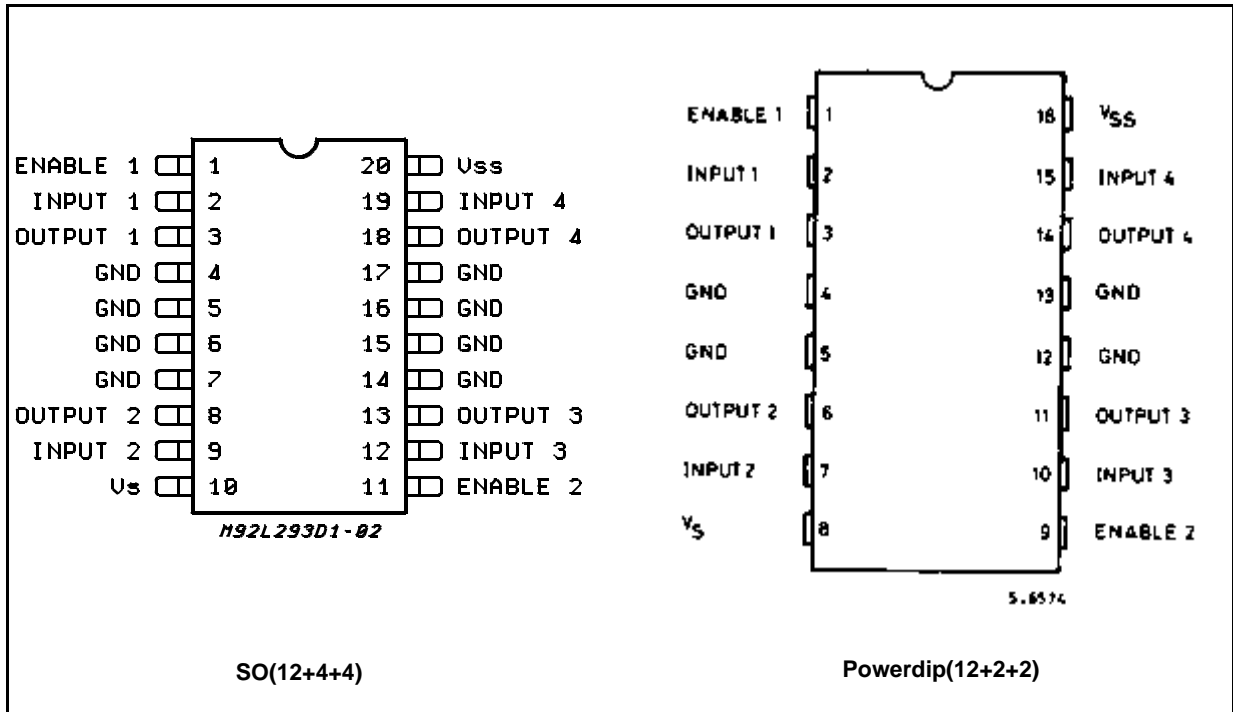


# L293D - L293DD

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>S</sub>	Supply Voltage	36	V
V <sub>SS</sub>	Logic Supply Voltage	36	V
V <sub>i</sub>	Input Voltage	7	V
V <sub>en</sub>	Enable Voltage	7	V
I <sub>o</sub>	Peak Output Current (100 μs non repetitive)	1.2	A
P <sub>tot</sub>	Total Power Dissipation at T <sub>pins</sub> = 90 °C	4	W
T <sub>stg</sub> , T <sub>j</sub>	Storage and Junction Temperature	- 40 to 150	°C

## PIN CONNECTIONS (Top view)



## THERMAL DATA

Symbol	Description	DIP	SO	Unit
R <sub>th j-pins</sub>	Thermal Resistance Junction-pins	max.	14	°C/W
R <sub>th j-amb</sub>	Thermal Resistance junction-ambient	max.	50 (*)	°C/W
R <sub>th j-case</sub>	Thermal Resistance Junction-case	max.	-	

(\*) With 6sq. cm on board heatsink.

**ELECTRICAL CHARACTERISTICS** (for each channel,  $V_S = 24\text{ V}$ ,  $V_{SS} = 5\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage (pin 10)		$V_{SS}$		36	V
$V_{SS}$	Logic Supply Voltage (pin 20)		4.5		36	V
$I_S$	Total Quiescent Supply Current (pin 10)	$V_i = L$ ; $I_O = 0$ ; $V_{en} = H$		2	6	mA
		$V_i = H$ ; $I_O = 0$ ; $V_{en} = H$		16	24	mA
		$V_{en} = L$			4	mA
$I_{SS}$	Total Quiescent Logic Supply Current (pin 20)	$V_i = L$ ; $I_O = 0$ ; $V_{en} = H$		44	60	mA
		$V_i = H$ ; $I_O = 0$ ; $V_{en} = H$		16	22	mA
		$V_{en} = L$		16	24	mA
$V_{IL}$	Input Low Voltage (pin 2, 9, 12, 19)		-0.3		1.5	V
$V_{IH}$	Input High Voltage (pin 2, 9, 12, 19)	$V_{SS} \leq 7\text{ V}$	2.3		$V_{SS}$	V
		$V_{SS} > 7\text{ V}$	2.3		7	V
$I_{IL}$	Low Voltage Input Current (pin 2, 9, 12, 19)	$V_{IL} = 1.5\text{ V}$			-10	$\mu\text{A}$
$I_{IH}$	High Voltage Input Current (pin 2, 9, 12, 19)	$2.3\text{ V} \leq V_{IH} \leq V_{SS} - 0.6\text{ V}$		30	100	$\mu\text{A}$
$V_{enL}$	Enable Low Voltage (pin 1, 11)		-0.3		1.5	V
$V_{enH}$	Enable High Voltage (pin 1, 11)	$V_{SS} \leq 7\text{ V}$	2.3		$V_{SS}$	V
		$V_{SS} > 7\text{ V}$	2.3		7	V
$I_{enL}$	Low Voltage Enable Current (pin 1, 11)	$V_{enL} = 1.5\text{ V}$		-30	-100	$\mu\text{A}$
$I_{enH}$	High Voltage Enable Current (pin 1, 11)	$2.3\text{ V} \leq V_{enH} \leq V_{SS} - 0.6\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{CE(sat)H}$	Source Output Saturation Voltage (pins 3, 8, 13, 18)	$I_O = -0.6\text{ A}$		1.4	1.8	V
$V_{CE(sat)L}$	Sink Output Saturation Voltage (pins 3, 8, 13, 18)	$I_O = +0.6\text{ A}$		1.2	1.8	V
$V_F$	Clamp Diode Forward Voltage	$I_O = 600\text{ nA}$		1.3		V
$t_r$	Rise Time (*)	0.1 to 0.9 $V_O$		250		ns
$t_f$	Fall Time (*)	0.9 to 0.1 $V_O$		250		ns
$t_{on}$	Turn-on Delay (*)	0.5 $V_i$ to 0.5 $V_O$		750		ns
$t_{off}$	Turn-off Delay (*)	0.5 $V_i$ to 0.5 $V_O$		200		ns

(\*) See fig. 1.

# L293D - L293DD

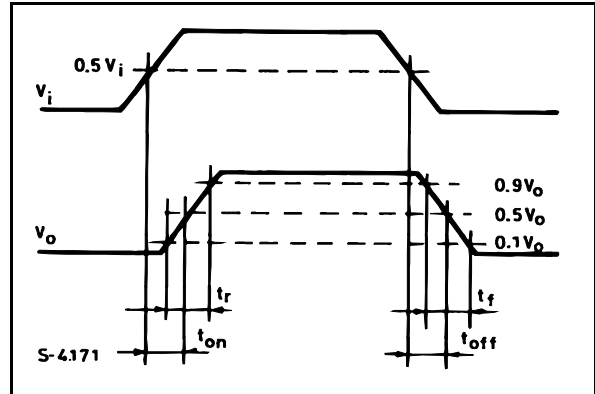
**TRUTH TABLE (one channel)**

Input	Enable (*)	Output
H	H	H
L	H	L
H	L	Z
L	L	Z

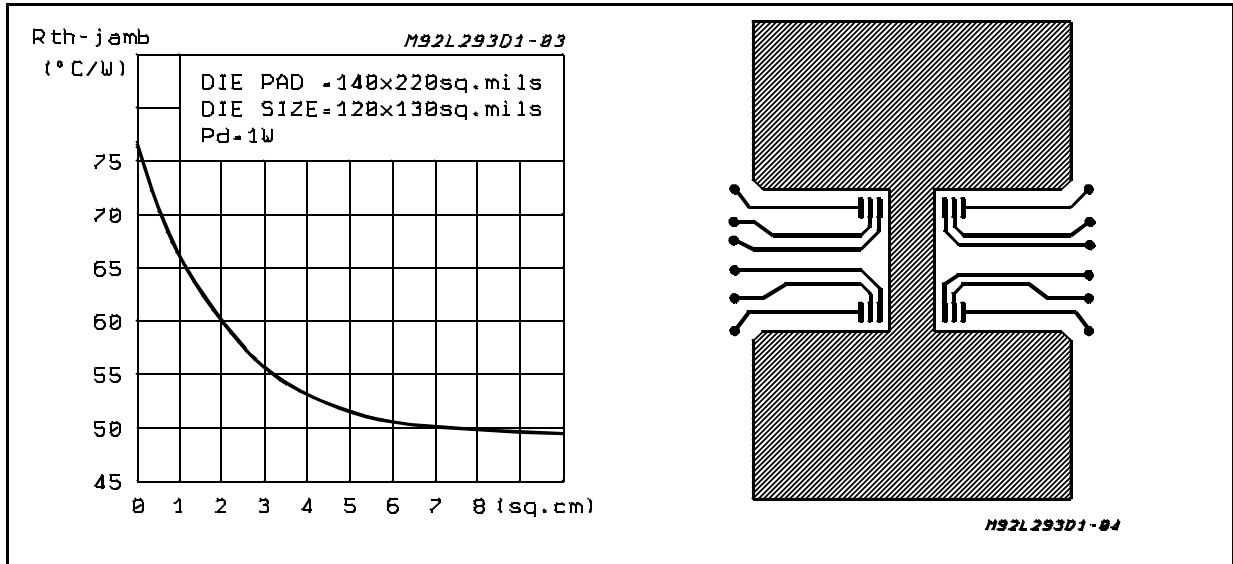
Z = High output impedance

(\*) Relative to the considered channel

**Figure 1: Switching Times**

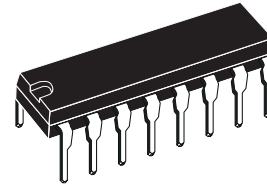


**Figure 2: Junction to ambient thermal resistance vs. area on board heatsink (SO12+4+4 package)**

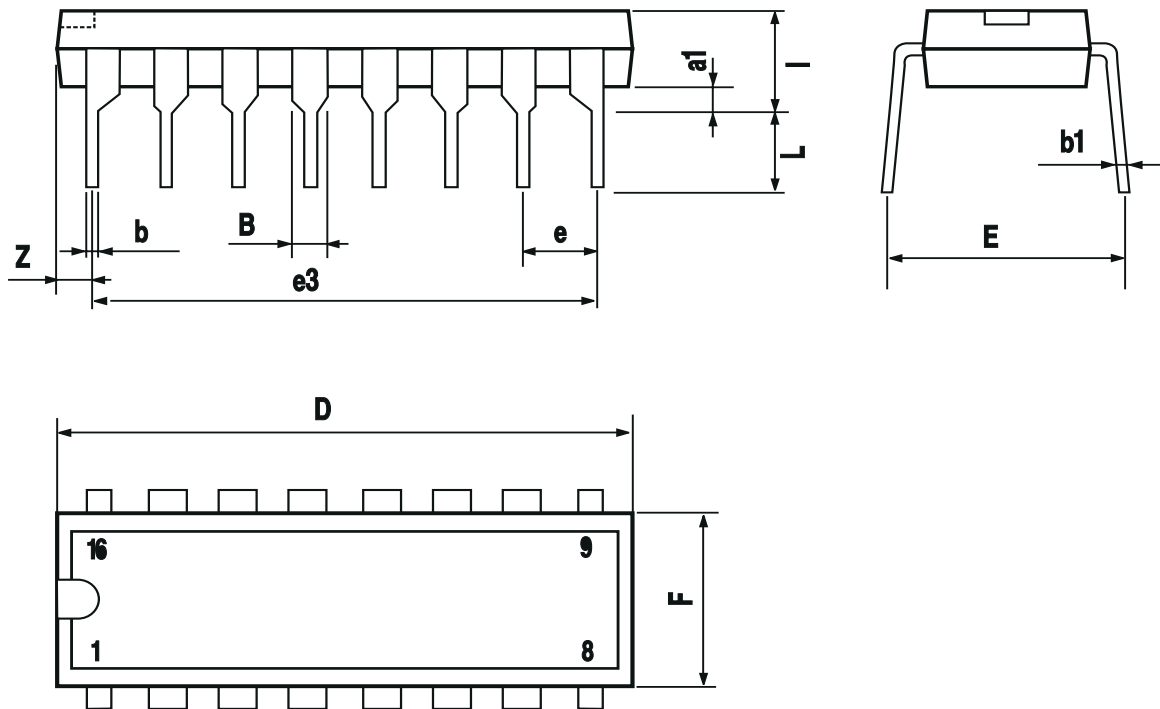


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.85		1.40	0.033		0.055
b		0.50			0.020	
b1	0.38		0.50	0.015		0.020
D			20.0			0.787
E		8.80			0.346	
e		2.54			0.100	
e3		17.78			0.700	
F			7.10			0.280
I			5.10			0.201
L		3.30			0.130	
Z			1.27			0.050

**OUTLINE AND MECHANICAL DATA**



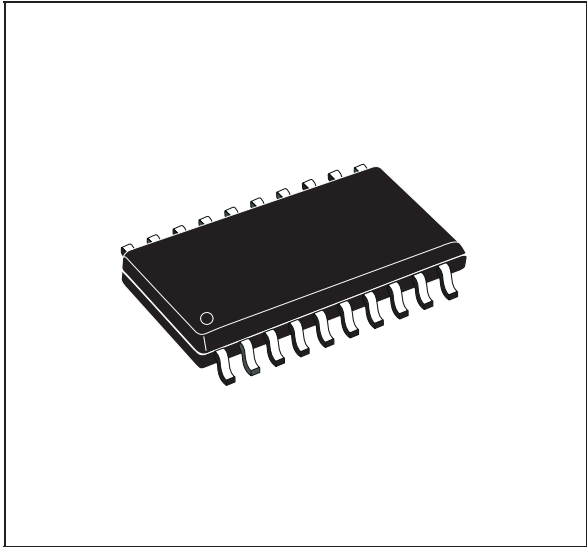
**Powerdip 16**



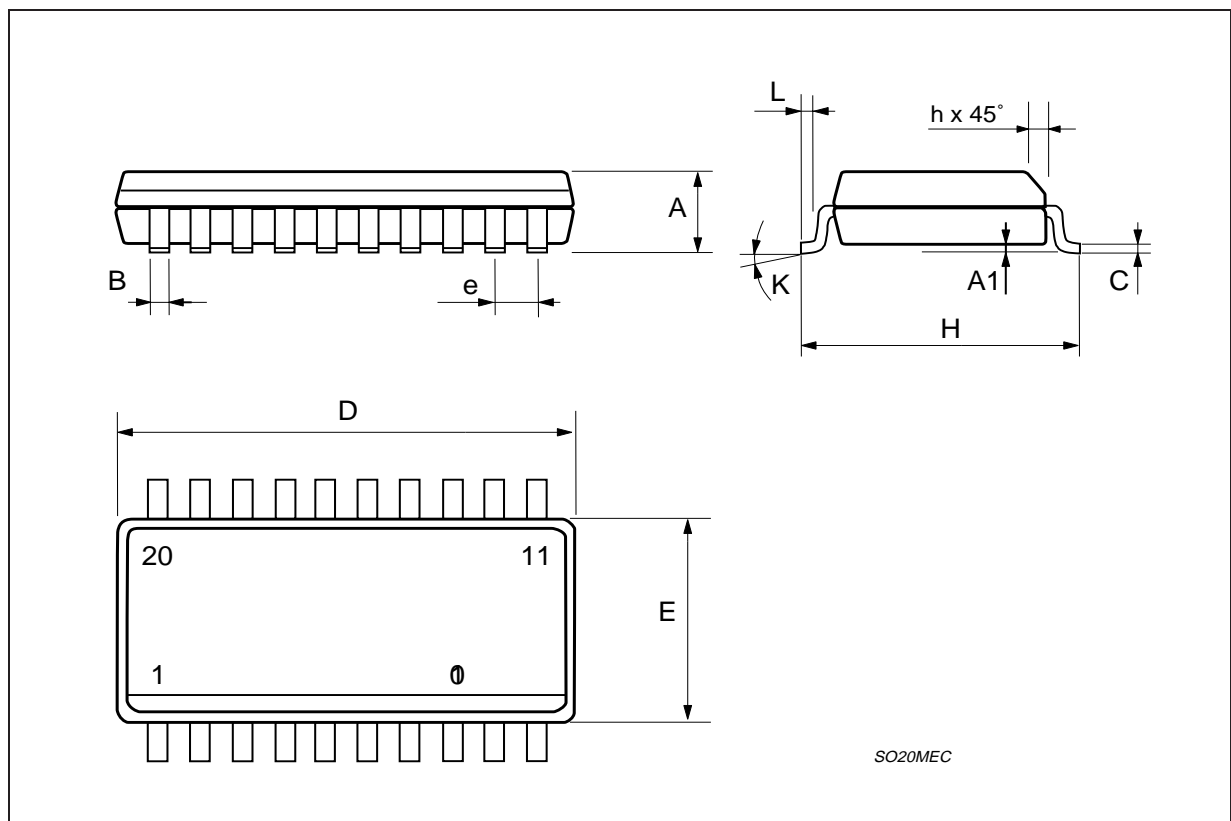
**L293D - L293DD**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
B	0.33		0.51	0.013		0.020
C	0.23		0.32	0.009		0.013
D	12.6		13	0.496		0.512
E	7.4		7.6	0.291		0.299
e		1.27			0.050	
H	10		10.65	0.394		0.419
h	0.25		0.75	0.010		0.030
L	0.4		1.27	0.016		0.050
K	0° (min.)8° (max.)					

**OUTLINE AND MECHANICAL DATA**



**SO20**



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics – Printed in Italy – All Rights Reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>