STP40NF10;ST;TO220;tranzystor; N-CHANNEL;50A;100V;150W;0.025R;Pbf

Dane techniczne:
Nazwa: STP40NF10
Typ tranzystora: unipolarny
Kierunek przewodnictwa: N-MOSFET
Prąd kolektora: 50A
Napięcie kolektor-emiter: 100V
Moc: 150W
Montaż: przewlekany(THT)
Obudowa: TO220
Producent: ST

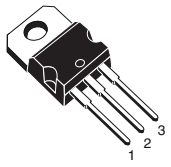
STP40NF10

N-channel 100 V, 0.025 Ω, 50 A TO-220 low gate charge STripFET™ II Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max.	I_D
STP40NF10	100 V	< 0.028 Ω	50 A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested



TO-220

Application

Switching applications

Description

This N-channel 100 V Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps allowing remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

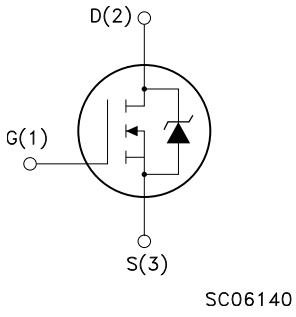


Table 1. Device summary

Order code	Marking	Package	Packaging
STP40NF10	P40NF10@	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	100	V
V_{GS}	Gate- source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	50	A
I_D	Drain current (continuous) at T_C = 100 °C	35	A
I_{DM} (2)	Drain current (pulsed)	200	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
	Derating factor	1	W/°C
dv/dt(3)	Peak diode recovery voltage slope	27	V/ns
E_{AS} (4)	Single pulse avalanche energy	385	mJ
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Max. operating junction temperature		

1. Limited by wire bonding
2. Pulse width limited by safe operating area
3. I_{SD} ≤50 A, di/dt ≤600 A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j ≤$T_{JMAX.}$
4. Starting T_j= 25 °C, I_D= 50 A, V_{DD}=25 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}a}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		80	A
I_{SDM} (1)	Source-drain current (pulsed)		-		320	A
V_{SD} (2)	Forward on voltage	I_{SD} = 50A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 50A, V_{DD} = 25V di/dt = 100A/µs, T_j = 150°C *(see Figure 16)*	-	80 250 6.4		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

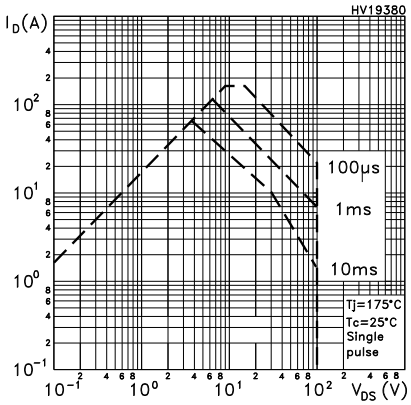


Figure 3. Thermal impedance for TO-220

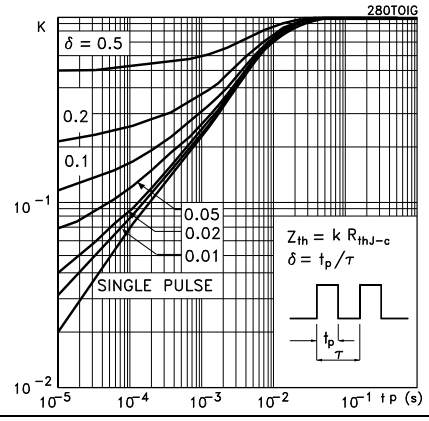


Figure 4. Output characteristics

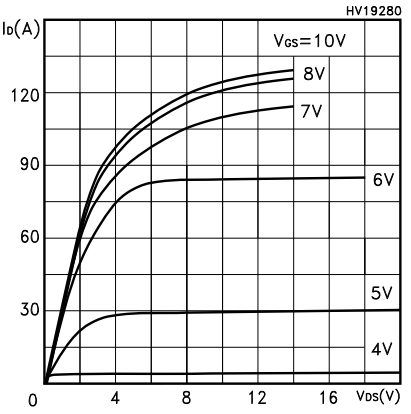


Figure 5. Transfer characteristics

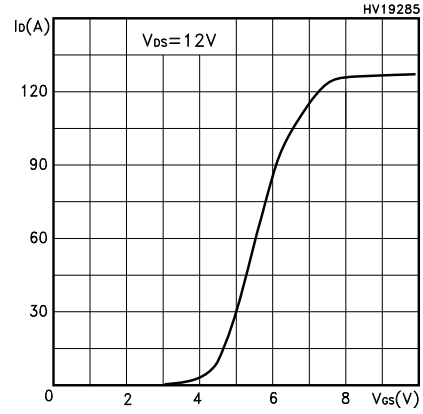


Figure 6. Transconductance

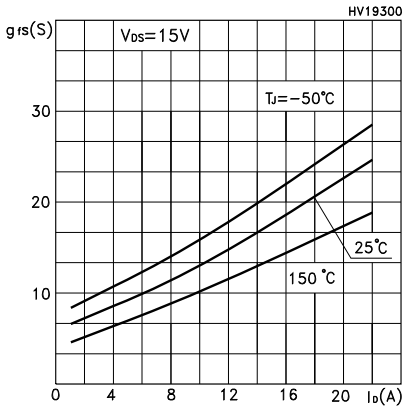


Figure 7. Static drain-source on resistance

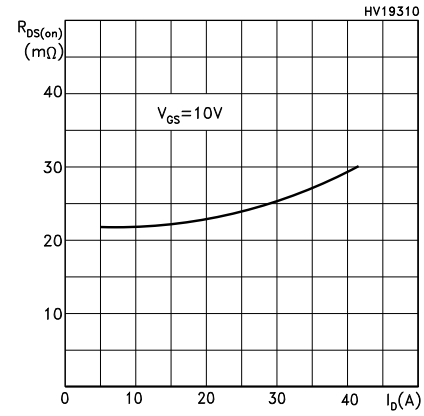


Figure 8. Gate charge vs. gate-source voltage

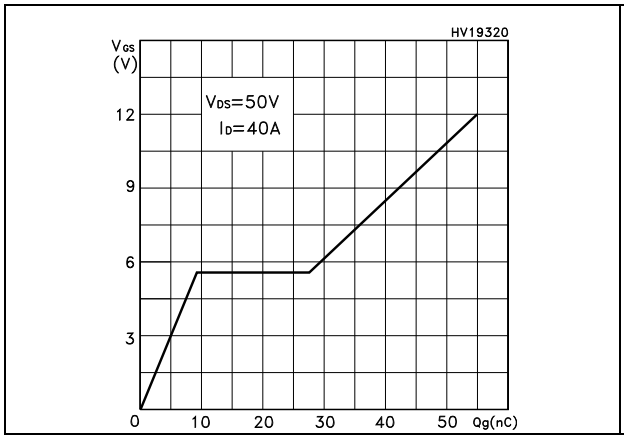


Figure 9. Capacitance variations

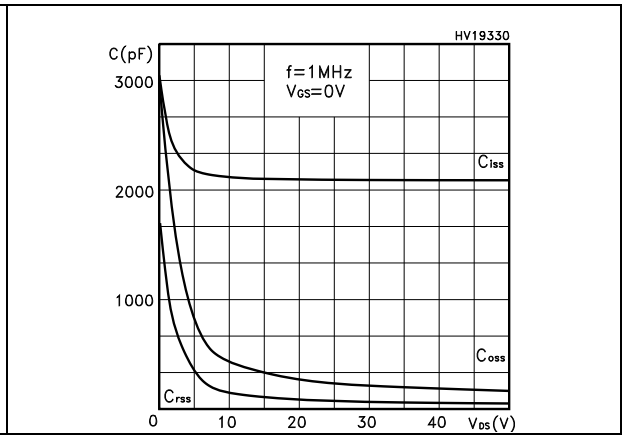


Figure 10. Normalized gate threshold voltage vs. temperature

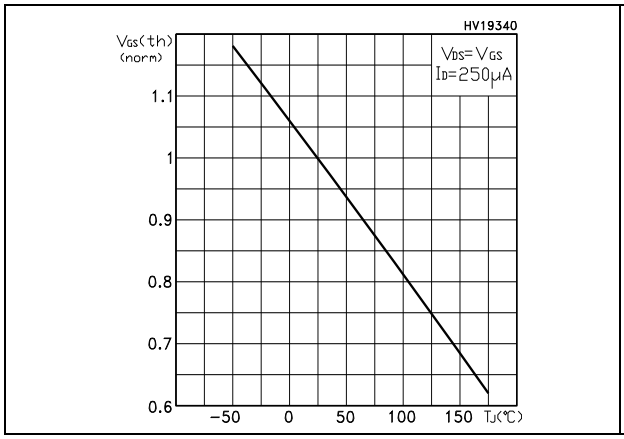


Figure 11. Normalized on resistance vs. temperature

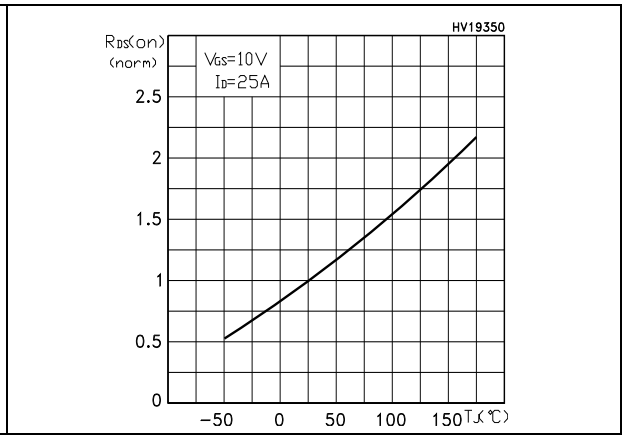


Figure 12. Source-drain diode forward characteristics

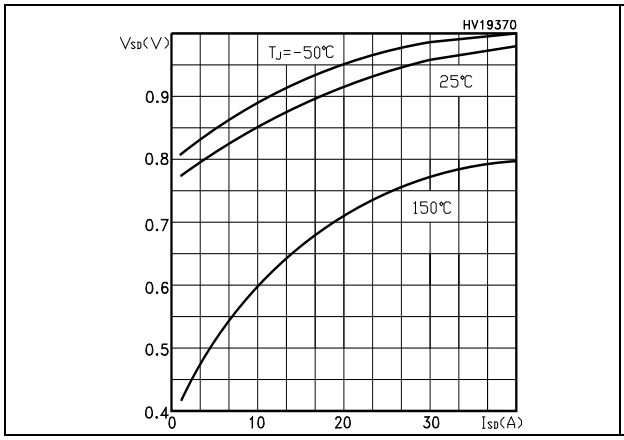
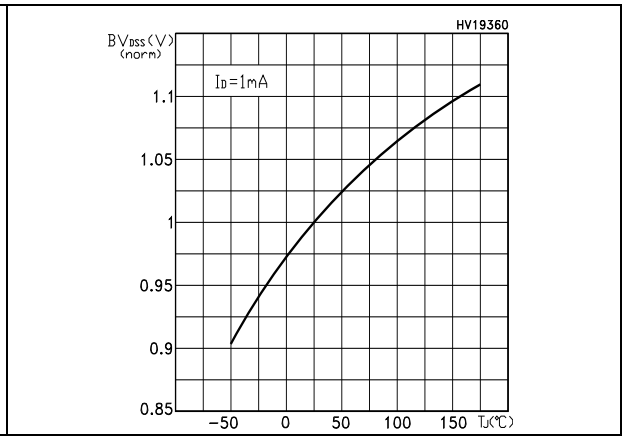


Figure 13. Normalized breakdown voltage vs. Tj



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
16-Dec-2004	1	First version.
17-Aug-2006	2	The document has been reformatted.
31-Jan-2007	3	Typo mistake on *Table 2*.
19-Sep-2007	4	Added DPAK.
10-Nov-2010	5	Removed DPAK.

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