

## CMOS BCD Rate Multiplier

High-Voltage Types (20-Volt Rating)

■ CD4527B is a low-power 4-bit digital rate multiplier that provides an output-pulse rate which is the clock-input-pulse rate multiplied by 1/10 times the BCD input. For example, when the BCD input is 8, there will be 8 output pulses for every 10 input pulses. This device may be used to perform arithmetic operations (add, subtract, divide, raise to a power), solve algebraic and differential equations, generate natural logarithms and trigonometric functions, A/D and D/A conversion, and frequency division.

For fractional multipliers with more than one digit, CD4527B devices may be cascaded in two different modes: the Add mode and the Multiply mode. (See Figs.12 and 15). In the Add mode,

$$\text{Output Rate} = (\text{Clock Rate}) \left[ \begin{array}{l} 0.1 \text{ BCD}_1 + 0.01 \text{ BCD}_2 + \\ 0.001 \text{ BCD}_3 + \dots \end{array} \right]$$

In the Multiply mode, the fraction programmed into the first rate multiplier is multiplied by the fraction programmed into the second one,

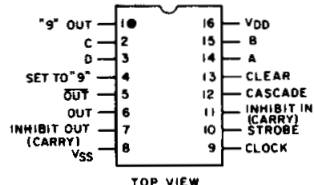
$$\text{e.g. } \frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \text{ or 36 output}$$

pulses for every 100 clock input pulses.

The CD4527B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

### Applications:

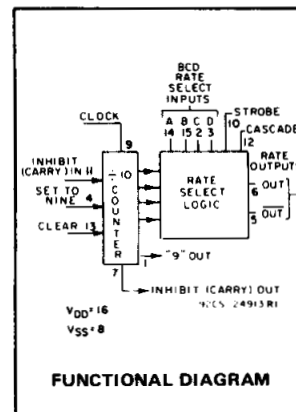
- Numerical control
- Instrumentation
- Digital filtering
- Frequency synthesis



TERMINAL ASSIGNMENT

### Features:

- Cascadable in multiples of 4-bits
- Set to "9" input and "9" detect output
- 100% test for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
  - 1 V at V<sub>DD</sub> = 5 V
  - 2 V at V<sub>DD</sub> = 10 V
  - 2.5 V at V<sub>DD</sub> = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13B, 'Standard Specifications for Description of 'B' Series CMOS Devices'



### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V <sub>DD</sub> )	-0.5V to +20V
Voltages referenced to V <sub>SS</sub> Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to V <sub>DD</sub> +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (P <sub>D</sub> ):	
For T <sub>A</sub> = -55°C to +100°C	500mW
For T <sub>A</sub> = +100°C to +125°C	Derate Linearly at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T <sub>A</sub> = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (T <sub>A</sub> )	-55°C to +125°C
STORAGE TEMPERATURE RANGE (T <sub>stg</sub> )	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

### RECOMMENDED OPERATING CONDITIONS AT T<sub>A</sub> = 25°C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V <sub>DD</sub> (V)	LIMITS		UNITS	
		Min.	Max.		
Supply Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)		3	18	V	
Set or Clear Pulse Width, t <sub>W</sub>	5	160	—	ns	
	10	90	—		
	15	60	—		
Clock Pulse Width, t <sub>W</sub>	5	330	—	ns	
	10	170	—		
	15	100	—		
Clock Frequency, f <sub>CL</sub>	5	—	1.2	MHz	
	10	dc	2.5		
	15	—	3.5		
Clock Rise or Fall Time, t <sub>rCL</sub> or t <sub>fCL</sub>	5, 10, 15	—	15	μs	
	5	100	—		ns
	10	40	—		
Inhibit In Setup Time, t <sub>SU</sub>	15	20	—	ns	
	5	240	—		ns
	10	130	—		
Inhibit In Removal Time, t <sub>REM</sub>	15	110	—	ns	
	5	150	—		ns
	10	80	—		
Set Removal Time, t <sub>REM</sub>	15	50	—	ns	
	5	60	—		ns
	10	40	—		
Clear Removal Time, t <sub>REM</sub>	15	30	—	ns	

# CD4527B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)					+25			
				-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0,5	5	5	5	150	150	-	0.04	5	μA
	-	0,10	10	10	10	300	300	-	0.04	10	
	-	0,15	15	20	20	600	600	-	0.04	20	
	-	0,20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I <sub>OL</sub> Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	0	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1, 9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1, 9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current I <sub>IN</sub> Max.		0,18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μA

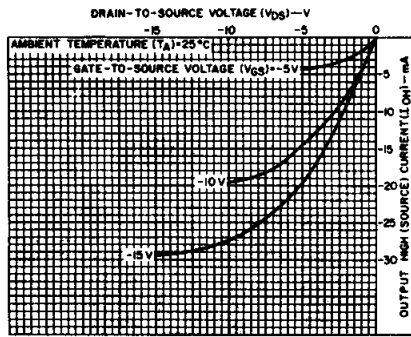


Fig. 3 - Typical output high (source) current characteristics.

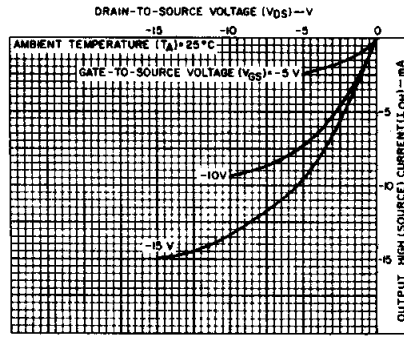


Fig. 4 - Minimum output high (source) current characteristics.

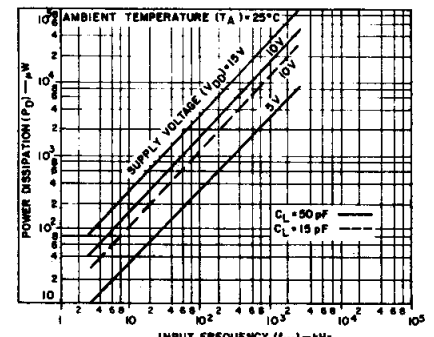


Fig. 5 - Typical dynamic power dissipation as a function of input frequency.

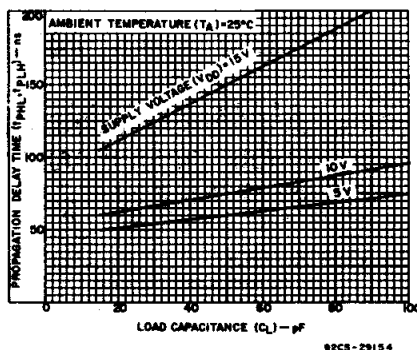


Fig. 6 - Typical propagation delay time as a function of load capacitance (Clock or Strobe to Out).

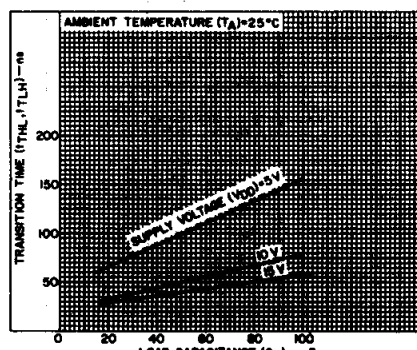


Fig. 7 - Typical transition time as a function of load capacitance.

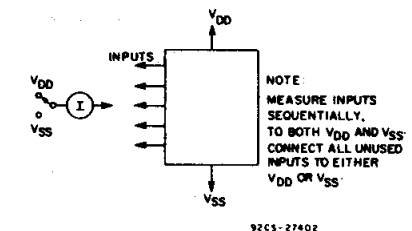


Fig. 8 - Input current test circuit.

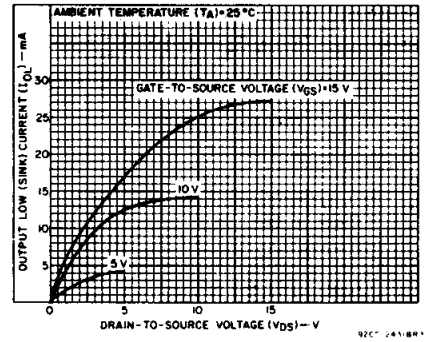


Fig. 1 - Typical output low (sink) current characteristics.

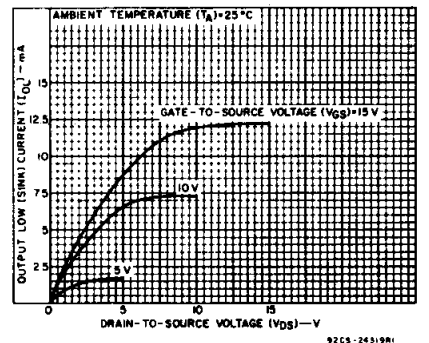


Fig. 2 - Minimum output low (sink) current characteristics.

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# CD4527B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C:**  
 Input t<sub>r</sub>, t<sub>f</sub> = 20 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS	
		V <sub>DD</sub> (V)	Min.	Typ.		Max.
Propagation Delay Time, t <sub>PHL</sub> , t <sub>PLH</sub> Clock to Out		5	—	110	ns	
		10	—	55		
		15	—	45		
Clock or Strobe to Out		5	—	150	ns	
		10	—	75		
		15	—	60		
Clock to Inhibit Out High Level to Low Level		5	—	320	ns	
		10	—	145		
		15	—	100		
Low Level to High Level		5	—	250	ns	
		10	—	100		
		15	—	75		
Clear to Out		5	—	380	ns	
		10	—	175		
		15	—	130		
Clock to "9" or "15" Out		5	—	300	ns	
		10	—	125		
		15	—	90		
Cascade to Out		5	—	90	ns	
		10	—	45		
		15	—	35		
Inhibit In to Inhibit Out		5	—	130	ns	
		10	—	60		
		15	—	45		
Set to Out		5	—	330	ns	
		10	—	150		
		15	—	110		
Transition Time, t <sub>THL</sub> , t <sub>TLH</sub>		5	—	100	ns	
		10	—	50		
		15	—	40		
Maximum Clock Frequency, f <sub>CL</sub>		5	1.2	2.4	MHz	
		10	2.5	5		
		15	3.5	7		
Minimum Clock Pulse Width, t <sub>w</sub>		5	—	165	ns	
		10	—	85		
		15	—	50		
Clock Rise or Fall Time, t <sub>rCL</sub> , t <sub>fCL</sub>		5	—	15	μs	
		10	—	15		
		15	—	15		
Minimum Set or Clear Pulse Width, t <sub>w</sub>		5	—	80	ns	
		10	—	45		
		15	—	30		
Minimum Inhibit In Setup Time, t <sub>SU</sub>		5	—	50	ns	
		10	—	20		
		15	—	10		
Minimum Inhibit In Removal Time, t <sub>REM</sub>		5	—	120	ns	
		10	—	65		
		15	—	55		
Minimum Set Removal Time, t <sub>REM</sub>		5	—	75	ns	
		10	—	40		
		15	—	25		
Minimum Clear Removal Time, T <sub>REM</sub>		5	—	30	ns	
		10	—	20		
		15	—	15		
Input Capacitance, C <sub>IN</sub>	Any Input		—	5	7.5	pF

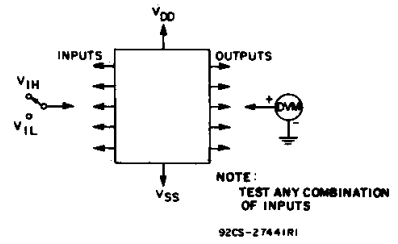


Fig. 9 - Input voltage test circuit.

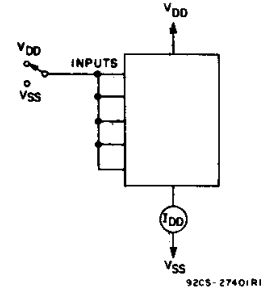


Fig. 10 - Quiescent device current test circuit.

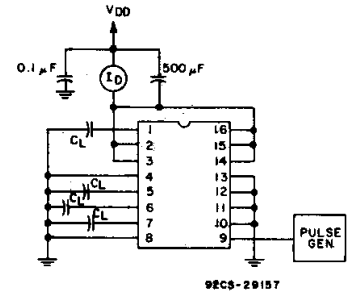


Fig. 11 - Dynamic power dissipation test circuit.

## APPLICATIONS

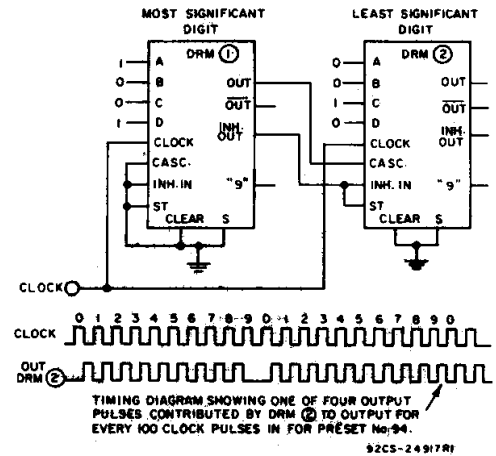


Fig. 12 - Two CD4527B's cascaded in the "Add" mode with a preset number

$$\text{of } 94 \left( \frac{9}{10} + \frac{4}{100} = \frac{94}{100} \right)$$

# CD4527B Types

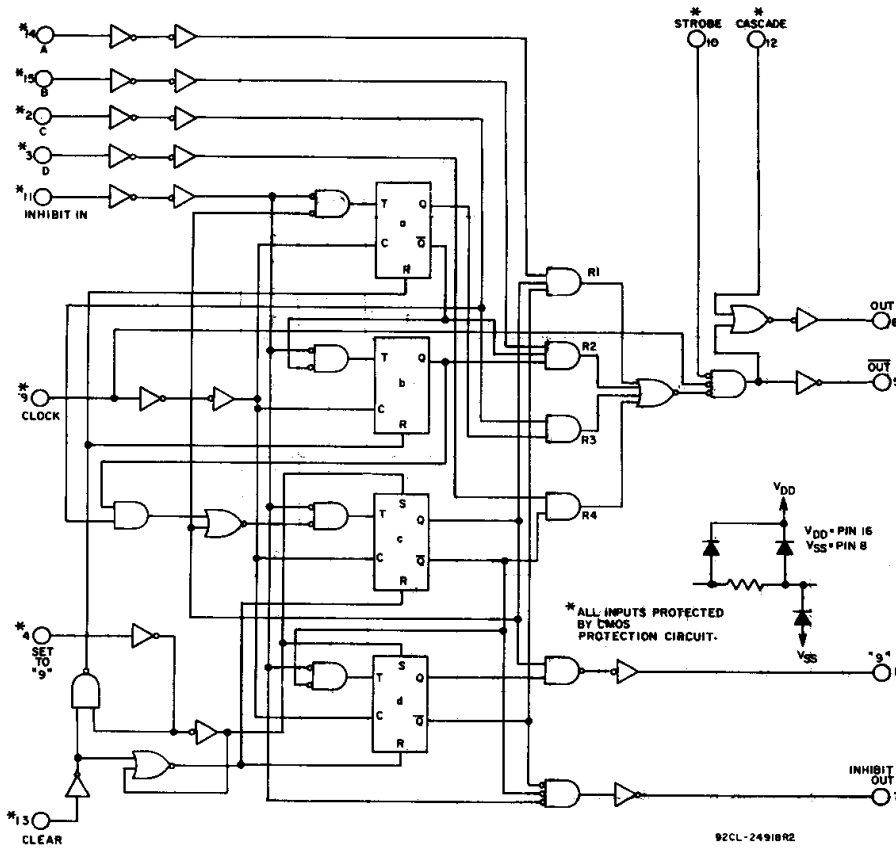


Fig. 13 - Logic diagram.

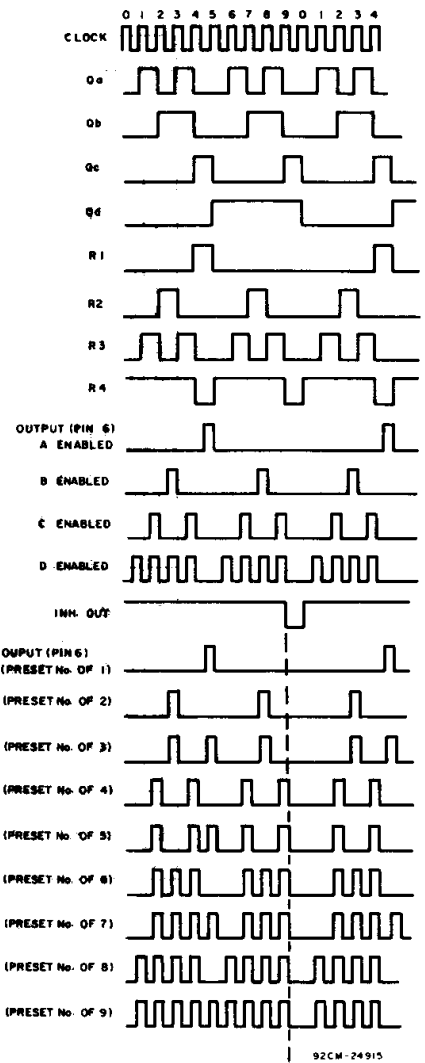
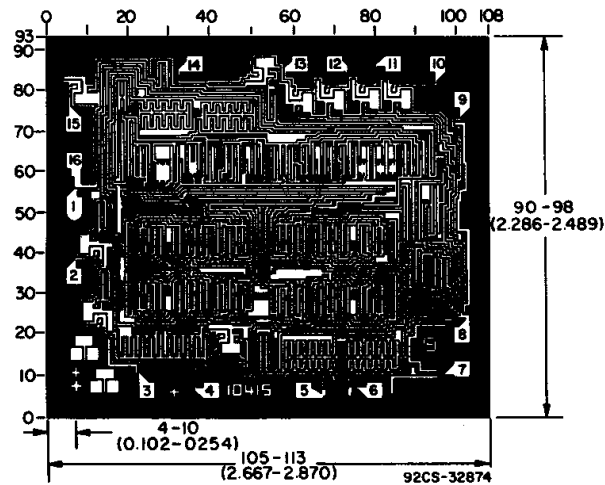


Fig. 14 - Timing diagram (See Logic Diagram).



Dimensions and Pad Layout for CD4527BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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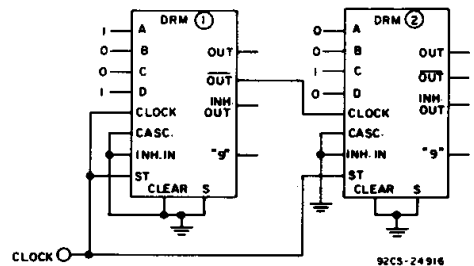


Fig. 15 - Two CD4527B's cascaded in the "Multiply" mode with a preset number

$$\text{of } 36 \left( \frac{9}{10} \times \frac{4}{10} = \frac{36}{100} \right)$$

## CD4527B Types

TRUTH TABLE

INPUTS										OUTPUTS			
Number of Pulses or Input Logic Level (0 = Low; 1 = High; X = Don't Care)										Number of Pulses or Output Logic Level (L = Low; H = High)			
D	C	B	A	CLK	INH IN	STR	CAS	CLR #	SET #	OUT	$\overline{\text{OUT}}$	INH OUT	"9" OUT
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	†	†	H	†
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

\* Output same as the first 16 lines of this truth table (depending on values of A, B, C, D).

† Depends on internal state of counter.

#Clear and Set Inputs should not be high at the same time; device draws increased quiescent current when in this non-valid state.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4527BE	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4527BE	<a href="#">Samples</a>
CD4527BEE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4527BE	<a href="#">Samples</a>
CD4527BNSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4527B	<a href="#">Samples</a>
CD4527BPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM527B	<a href="#">Samples</a>
CD4527BPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM527B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4527BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4527BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4527BNSR	SO	NS	16	2000	853.0	449.0	35.0
CD4527BPWR	TSSOP	PW	16	2000	853.0	449.0	35.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

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